

REMARKS

Claims 1-20 are pending in the Application. Claim 1 is an independent claim and claims 2-7 and 19 depend therefrom. Claim 8 is an independent claim and claims 9-13 and 20 depend therefrom. Claim 14 is an independent claim and claims 15-18 depend therefrom. Claims 1, 8 and 14 are currently amended. Claims 15, 19 and 20 are canceled. The Applicant respectfully requests that the application be reconsidered in view of foregoing amendments and the following remarks.

Rejections Under 35 U.S.C. §102(e) - MacInnis

Claims 1-20 were rejected under 35 U.S.C. §102(e) as being anticipated by MacInnis et al. (U.S. Pub. No. 2003/0185306, hereinafter "MacInnis"). Without acknowledging that MacInnis qualifies as prior art under 35 U.S.C. §102(e), the Applicant respectfully traverses the rejections for at least the following reasons.

With regard to the anticipation rejections, MPEP 2131 states, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). MPEP 2131 also states, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Regarding claim 1, the Applicant respectfully submits that the cited sections of MacInnis fail to teach, suggest, or disclose, for example, "a host processor for providing an indication to the video decoder indicating the particular encoding standard, wherein the video decoder for decoding the video data encoded with the particular standard and at least performing picture

level processing, is discrete from the host processor,” as set forth in Applicant’s independent claim 1.

MacInnis discloses “[p]icture level processing, including sequence headers, GOP headers, picture headers, time stamps, macroblock-level information except the block coefficients, and buffer management, **are performed directly and sequentially by the core processor 302...**” (MacInnis, Paragraph [0030]). Thus, because the cited sections of MacInnis teaches that the core processor performs picture level processing, the sections of MacInnis cited by the final Office Action (e.g., Figs. 1-3, Abstract, [0002], [0011], [0030], [0031], [0040], [0044], [0065] and [0083]) cannot disclose “a host processor for providing an indication to the video decoder indicating the particular encoding standard, wherein **the video decoder** for decoding the video data encoded with the particular standard and at least **performing picture level processing, is discrete from the host processor,**” as set forth in Applicant’s independent claim 1. Because the Office Action has failed to show “each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference” as required for an anticipation rejection under MPEP 2131, the rejection of claim 1 under 35 U.S.C. § 102(e) cannot be maintained.

Therefore, for at least the above stated reasons, Applicant respectfully submits that the cited sections of the MacInnis reference fails to teach, suggest, or disclose Applicant’s invention as set forth in claim 1. The Applicant believes that claim 1 is allowable over MacInnis. Applicant respectfully submits that claim 1 is an independent claim, and that claims 2-7 depend either directly or indirectly from independent claim 1. Because claims 2-7 depend from claim 1, Applicant respectfully submits that claims 2-7 are allowable over the MacInnis reference, as well. The Applicant respectfully requests, therefore, that the rejection of claims 1-7 under U.S.C. §102(e), be withdrawn.

Regarding claim 8, the Applicant respectfully submits that the cited sections of MacInnis fail to teach, suggest, or disclose, for example, “receiving an indication from a host processor by a video decoder indicating the particular encoding standard, wherein the video decoder at least performs picture level processing and is discrete from the host processor,” as set forth in Applicant’s independent claim 8.

As discussed above, MacInnis discloses “**picture level processing**, including sequence headers, GOP headers, picture headers, time stamps, macroblock-level information except the block coefficients, and buffer management, **are performed directly and sequentially by the core processor 302...**” (MacInnis, Paragraph [0030]). Thus, because the cited sections of MacInnis teach that the core processor performs the picture level processing, the sections of MacInnis cited by the final Office Action (e.g., Figs. 1-3, Abstract, [0002], [0011], [0030], [0031], [0040], [0044], [0065] and [0083]) cannot disclose “providing an indication from a host processor to a video decoder indicating the particular encoding standard to the video decoder, **wherein the video decoder at least performs picture level processing and is discrete from the host processor,**” as set forth in Applicant’s independent claim 8. Because the Office Action has failed to show “each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference” as required for an anticipation rejection under MPEP 2131, the rejection of claim 8 under 35 U.S.C. § 102(e) cannot be maintained.

Therefore, for at least the above stated reasons, Applicant respectfully submits that the cited sections of the MacInnis reference fails to teach, suggest, or disclose Applicant’s invention as set forth in claim 8. The Applicant believes that claim 8 is allowable over MacInnis. Applicant respectfully submits that claim 8 is an independent claim, and that claims 9-13 depend either directly or indirectly from independent claim 8. Because claims 9-13 depend from claim 8, Applicant respectfully submits that claims 9-13 are allowable over the MacInnis reference, as well. The Applicant respectfully requests, therefore, that the rejection of claims 8-13 under U.S.C. §102(e), be withdrawn.

Regarding claim 14, the Applicant respectfully submits that MacInnis fails to teach, suggest, or disclose, for example, “wherein the processor loads the code memory after receiving an indication from a discrete host processor indicating the particular encoding standard,” as set forth in Applicant’s independent claim 14.

MacInnis discloses “[t]he hardware accelerators are programmed or **configured by the core processor 302** to operate according to the appropriate encoding/decoding format. ... The **core processor programs registers in each module to modify the operational behavior of the module.**” (MacInnis, Paragraph [0083, last 14 lines] (emphasis added)). Thus, because the cited sections of MacInnis teaches that the core processor configures the hardware accelerators by programming the hardware accelerators’ registers, the sections of MacInnis cited in the final Office Action (e.g., Figs. 1-2, Abstract, [0002], [0065], [0083, last 14 lines]) cannot disclose “wherein **the processor loads the code memory after receiving an indication from a discrete host processor indicating the particular encoding standard,**” as set forth in Applicant’s independent claim 14. Because the Office Action has failed to show “each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference” as required for an anticipation rejection under MPEP 2131, the rejection of claim 14 under 35 U.S.C. § 102(e) cannot be maintained.

Therefore, for at least the above stated reasons, Applicant respectfully submits that the cited sections of the MacInnis reference fail to teach, suggest, or disclose Applicant’s invention as set forth in claim 14. The Applicant believes that claim 14 is allowable over MacInnis. Applicant respectfully submits that claim 14 is an independent claim, and that claims 16-18 depend either directly or indirectly from independent claim 14. Because claims 16-18 depend from claim 14, Applicant respectfully submits that claims 16-18 are allowable over the MacInnis reference, as well. The Applicant respectfully requests, therefore, that the rejection of claims 14, 16-18 under U.S.C. §102(e), be withdrawn.

Appl. No. 10/775,652
Resp. to Office Action mailed July 9, 2008
Response dated October 9, 2008

Final Matters

The Office Action makes various statements regarding claims 1-20, 35 U.S.C. § 102(e), the MacInnis reference, etc. that are now moot in view of the above amendments and/or arguments. Thus, the Applicant will not address all of such statements at the present time. However, the Applicant expressly reserves the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

Applicant reserves the right to argue additional reasons supporting the allowability of claims 1-14 and 16-18 should the need arise in the future.

Appl. No. 10/775,652
Resp. to Office Action mailed July 9, 2008
Response dated October 9, 2008

CONCLUSION

Applicant respectfully submits that all of claims 1-14 and 16-18 are in condition for allowance, and requests that the application be passed to issue.

Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Dated: October 9, 2008

Respectfully submitted,

/Philip Henry Sheridan/
Philip Henry Sheridan
Reg. No. 59,918

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
(T) 312 775 8000
(F) 312 775 8100